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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,221	08/06/2001	Yongdong Zhao	5694-00200	8970

7590 08/10/2005

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EXAMINER	
MARTIN, NICHOLAS A	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 09/923,221	Applicant(s) ZHAO ET AL.	
	Examiner Nicholas Martin	Art Unit 2154	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 19 July 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☒ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). 01/05/04
13. ☐ Other: _____.

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Continuation of 11. does NOT place the application in condition for allowance because:

Applicants' arguments filed on 07/19/05 have been fully considered but they are not persuasive.

As per remarks, Applicants' argued that (1) Welin does not disclose a memory coupled to a cell processing unit and configured to store one or more policy parameters and rollover data for each of the communication channels, wherein the rollover data comprises an indication of a rollover relationship between the timer value and one of the policy parameters for each of the communication channels.

As to point (1), Welin teaches a memory coupled to a cell processing unit and configured to store one or more policy parameters (Paragraphs [0086] "...a computer box including one or more information storage devices...with microprocessor(s), digital signal processor(s), volatile memory..."; [0092] "Each DSP suitably has associated memory...") and rollover data for each of the communication channels, wherein the rollover data comprises an indication of a rollover relationship between the timer value and one of the policing parameters for each of the communication channels (Paragraphs [0015-0016] "...includes computing for each of said received packets respective deadline intervals and ordering processing...according to perspective deadline intervals...packet control establishing an egress scheduling list structure and operations in the processor circuit that extract packet deadline intervals..."; [0017] "...a single-chip circular time differencing integrated circuit has a storage for values representative of the time of two events. An adder/subtractor coupled to the storage generates an electronic difference (delta) and delivers the difference value into storage..."; [0058] "...establishes a temporal relationship between the time of arrival of a packet and the time it has to be decoded and added to the data stream (placed in the buffer)..."; [0154] "...egress buffer reserves for several channels..."; [0518-0520]; [0547-548] "...select a desirable clock rate and corresponding clock cycle period and an estimate of the largest interval of time that needs to be maintained by the stream...provides the required clock range..."; [0550]; [0558] "...circular time the two values can possibly straddle clock modulus time boundary, producing false results, i.e., a form of rollover error.").

As per remarks, Applicants' argued that (2) Welin does not disclose that for each received incoming data cell, the cell processing unit is configured to assign an arrival time from the timer value and compare the received incoming data cell's arrival time to one of the one or more policing parameters for the received incoming data cell's communication channel to determine if the received incoming data cell is conforming or non-conforming to a rate for the communication channel.

As to point (2), Welin teaches that for each incoming data cell, the cell processing unit is configured to assign an arrival time from the timer value and compare the received incoming data cell's arrival time to one of the one or more policing parameters for the received incoming data cell's communication channel (Paragraphs [0017] "...a single-chip circular time differencing integrated circuit has a storage for values representative of the time of two events. An adder/subtractor coupled to the storage generates an electronic difference (delta) and delivers the difference value into storage..."; [0058] "...establishes a temporal relationship between the time of arrival of a packet and the time it has to be decoded and added to the data stream (placed in the buffer)..."; [0154] "...egress buffer reserves for several channels..."; [0158] "...there is an optimal moment to start the first frame. That moment is related to the arrival time of the first packet..."; [0518-0520]; [0547-548] "...select a desirable clock rate and corresponding clock cycle period and an estimate of the largest interval of time that needs to be maintained by the stream...provides the required clock range..."; [0550]; [0555]) to determine if the received incoming data cell is conforming or non-conforming to a rate for the communication channel (Paragraphs [0231] "...decoded to prevent it from being lost due to late arrival or unnecessarily-delayed handling in the computer."; [0253] "...when the computer receives the packets...some packets may be too late or lost..."; [0264]; [0555-0557]).

As per remarks, Applicants' argued that (3) Welin does not teach that the cell processing unit is configured to access rollover data for the received incoming data cell's communication channel to account for the rollover relationship when comparing the arrival time to one or more policing parameters.

As to point (3), Welin teaches that the cell processing unit is configured to access rollover data fro the received incoming data cell's communication channel to account for the rollover relationship when comparing the arrival time to one or more policing parameters (Paragraphs [0017] "...a single-chip circular time differencing integrated circuit has a storage for values representative of the time of two events. An adder/subtractor coupled to the storage generates an electronic difference (delta) and delivers the difference value into storage..."; [0058] "...establishes a temporal relationship between the time of arrival of a packet and the time it has to be decoded and added to the data stream (placed in the buffer)..."; [0080] "...link list tells the system which packets to decode first, in order of their deadline number...accesses the cell at to top of the queue...detects what process to use, and for what channel..."; [0140] "...arriving packet, the process accesses addresses...computes the current reserve for that channel"; [0146-0147] ".....access to the deadline time, by which the packet's data is inserted into the egress buffer...the packets in the queue for decoding are sorted with respect to their deadline times. The values of those reserves are accessible for each packet in the queue [0154] "...egress buffer reserves for several channels..."; [0158] "...there is an optimal moment to start the first frame. That moment is related to the arrival time of the first packet..."; [0518-0520]; [0547-548] "...select a desirable clock rate and corresponding clock cycle period and an estimate of the largest interval of time that needs to be maintained by the stream...provides the required clock range..."; [0550]; [0558] "...circular time the two values can possibly straddle clock modulus time boundary, producing false results, i.e., a form of rollover error.").

As per remarks, Applicants' argued that (4) Welin and/or Fahmi do not teach or suggest that the rollover data is configured to indicate for each communication channel whether or not the timer value and theoretical arrival time are in the same rollover phase.

As to point (4), Fahmi teaches that the rollover data is configured to indicate for each communication channel whether or not the timer value and theoretical arrival time are in the same rollover phase (Col. 1, lines 59-65 "...determining if a theoretical arrival time TAT is less than an arrival time for a cell..."; Col. 2, lines 62-67; Col. 4, lines 1-5, 19-29, 53-58 "...update flag has an input from clock which provides an output at typically about 1 second intervals...rollover period of the time-of-arrival rollover period of the time-of-arrival counter...stored the values of the theoretical arrival time, TAT, and the increment, I. ...Upon completion of processing time for the cell arriving just after rollover, during which the processor suspends processing of the cell arrival time, a reset signal is sent...which

resets the latter and removes the flag input). Welin teaches that the values are in the same rollover phase (Paragraphs [0058] "...establishes a temporal relationship between the time of arrival of a packet and the time it has to be decoded and added to the data stream (placed in the buffer)..."; [0130-0134] "...measures of time expressed as the number of clock cycles. Assuming that the clock is the sampling clock, the number of time units in that region are the same."; [0373] "Each packet, as it arrives, contains 80 samples. A phase lock loop enhances clock recovery to reconstitute clock for resampling at the receiver...").

As per remarks, Applicants' argued that (5), Welin and/or Fahmi do not teach or suggest a memory configured to store operations and maintenance data indicating connection availability information for each communication channel.

As to point (5), Welin teaches a memory configured to store operations and maintenance data indicating connection availability information for each communication channel (Paragraphs [0256] "...updates the channel records...acting as a source of maintenance..."; [0318] "Maintenance of a queue...from the DMA hardware. The DMA is programmed for the ingress side to continually put data from a line into the buffer or buffers..."; [0259]; [0310]; [0620] "...add memory and a control program...in normal operation or during maintenance...VoIP control and TCP/UDP/IP packet network protocol stack and an ingress/egress control block...").

As per remarks, Applicants' argued that (6) Welin and/or Fahmi in further view of "Official Notice" do not teach or suggest a network device wherein a timer rollover phase indicator comprises a global register bit configured to be toggled each time the timer value rolls over.

As to point (6), Welin teaches a timer rollover phase indicator comprises a global register bit configured to be toggled each time the timer value rolls over (Paragraph [0194] "...DMA registers are readily looked up...when a packet arrives is determinable in terms of number of samples until the boundary."; [0329] "...process resets the boundary, schedules the ingress, and updates all of the egress deadlines...checks whether a new egress packet flag is set...leads to execution of the ISR for new packet to create new cell..."; [0417] "...register is accessed by a scheduler for that information stored therein for use in determining how to schedule packets, and whether to preempt...first initialize a register and then transfer and decode...20 bits from a frame...data in an egress packet queue...a break process initiates a call to scheduler. Also a break process updates a register..."; [0418] "...scheduler...takes care of any just-arrived packets...20 more bits, followed by another break process..."; [0419]; [0542]; [0550-0555]).

As per remarks, Applicants' argued that (7) Welin and/or Fahmi in further view of "Official Notice" do not teach or suggest any value that indicates that the theoretical arrival time value for a communication channel is ahead, behind or in the same rollover phase as the timer value.

As to point (7), Fahmi teaches any value that indicates that the theoretical arrival time value for a communication channel is ahead, behind or in the same rollover phase as the timer value (Col. 4, lines 1-5 "...update flag has an input from clock which provides an output at typically about 1 second intervals...rollover period of the time-of-arrival rollover period of the time-of-arrival counter...", lines 10-29 "...n-bit parallel output passes...in response to the arrival of a cell arrival signal...arrival signal is issued upon completion of arrival of a octets of data. The time of arrival on bus line is applied to an input of processor giving to processor the time of arrival for each cell. Processor stores this value in RAM memory. Processor also has stored the values of the theoretical arrival time, TAT... Upon completion of processing time for the cell arriving just after rollover, during which the processor suspends processing of the cell arrival time, a reset signal is sent...which resets the latter and removes the flag input", lines 53-58). Welin teaches that the values are in the same rollover phase (Paragraphs [0058] "...establishes a temporal relationship between the time of arrival of a packet and the time it has to be decoded and added to the data stream (placed in the buffer)..."; [0130-0134] "...measures of time expressed as the number of clock cycles. Assuming that the clock is the sampling clock, the number of time units in that region are the same."; [0373] "Each packet, as it arrives, contains 80 samples. A phase lock loop enhances clock recovery to reconstitute clock for resampling at the receiver...").